CLAIMS

What is claimed is:

1. An apparatus to correct a reference voltage (Vref) of a digital device to input/output digital data, comprising:

a Vref setup selecting part selecting a correction of the Vref;

a Vref adjusting circuit adjusting the Vref of the digital device; and

a Vref control storing part storing a Vref control program to change setup of the Vref adjusting circuit to vary the Vref output from the Vref adjusting circuit to be varied, detecting a transmission state of the digital data of the digital device, determining an optimum setup of the Vref adjusting circuit to allow error bits of the digital data to be minimized, and setting up the Vref adjusting circuit according to selection of the Vref correction through the Vref setup selecting part.

2. The apparatus for correcting the reference voltage according to claim 1, wherein the Vref control program comprises a BIOS program.

3. The apparatus to correct the reference voltage according to claim 1, wherein the Vref adjusting circuit comprises:

an adjustable resistor, and

a fixed resistor to generate the Vref correction by dividing a main supply voltage of the digital device, wherein the Vref control program changes a resistance value of the adjustable resistor according to the selection of the Vref correction through the Vref setup selecting part, detects the transmission state of the digital data of the digital devices, determines an optimum resistance value of the adjustable resistor to allow the error bits of the digital data to be minimized, and sets up the resistance value of the adjustable resistor as the optimum resistance value.

4. The apparatus for correcting the reference voltage according to claim 2, wherein the Vref adjusting circuit comprises:

an adjustable resistor, and

a fixed resistor to generate the Vref correction by dividing a main supply voltage of the digital device, wherein the Vref control program changes a resistance value of the adjustable resistor according to the selection of the Vref correction through the Vref setup selecting part, detects the transmission state of the digital data of the digital devices, determines an optimum resistance value of the adjustable resistor to allow the error bits of the digital data to be minimized, and sets up the resistance value of the adjustable resistor as the optimum resistance value

5. The apparatus for correcting the reference voltage according to claim 1, further comprising:

a Vref optimum setup storing part to store data of optimum setup condition of the Vref adjusting circuit.

6. An apparatus to correct a reference voltage, Vref, comprising:

a first digital device and a second digital device inputting/outputting digital data via a bus;

an adjustable resistor providing a main supply voltage VDD;

a fixed resistor, wherein the adjustable resistor and the fixed resistor generate a Vref correction by dividing the main supply voltage VDD;

a Vref setup selecting part selecting the Vref correction; and

a Vref controller changing a resistance value of the adjustable resistor according to a selection of the Vref correction through the Vref setup selecting part, determining an optimum resistance value of the adjustable resistor, and outputting an optimum Vref correction.

7. The apparatus to correct the reference voltage according to claim 6, wherein the Vref controller analyzes signals input/output between the first and second digital devices by transmitting through the bus a digital signal corresponding to the change of the resistance value of the adjustable resistor.

8. The apparatus to correct the reference voltage according to claim 7, wherein the Vref controller confirms a transmission state of the digital signal according to the change of the resistance value of the adjustable resistor and confirms if error bits occur in the digital signal.

9. The apparatus to correct the reference voltage according to claim 6, wherein the Vref controller calculates the optimum resistance value where the occurrence of the error bits is low and sets up the resistance value of the adjustable resistor as the calculated optimum resistance value.

10. The apparatus to correct the reference voltage according to claim 6, further comprising:

an optimum resistance storing part storing the optimum resistance value.

11. The apparatus to correct the reference voltage according to claim 6, wherein the Vref controller comprises a BIOS program.

12. A method to correct a reference voltage, Vref, of digital device having a Vref adjusting circuit to adjust the Vref, comprising:

selecting a reference voltage correction;

changing a setup of the Vref adjusting circuit to vary the Vref;

detecting a transmission state of digital data output from the digital device, according to the changed setup of the Vref adjusting circuit;

determining an optimum setup of the Vref adjusting circuit to allow error bits of the digital data to be minimized; and

setting up the Vref adjusting circuit according to the optimum setup.

13. A method to correct a reference voltage, Vref, between first and second digital devices, comprising:

selecting a Vref correction via a BIOS setup menu;

adjusting a resistance value;

loading a digital signal corresponding to a change of the resistance value through a bus;

confirming a state that the digital signal is transmitted;

calculating an optimum resistance value where a Vref correction is output to minimize error bits of the transferred digital signal;

setting up the resistance value as a calculated optimum resistance value; and

storing the optimum resistance value.

14. The method to correct the reference voltage according to claim 13, further comprising:

analyzing signals input/output between the first and second digital devices by transmitting through the bus the digital signal corresponding to the change of the resistance value.

15. The method to correct the reference voltage according to claim 13, wherein the confirmation of the state of transmission of the digital signal according to the change of the resistance value.

16. The method to correct the reference voltage according to claim 15, further comprising:

confirming whether error bits occur in the digital signal;

calculating the optimum resistance value where the occurrence of the error bits is low; and

setting up the resistance value as the calculated optimum resistance value.